unpatentable over Maesako et al. (U.S. Patent No. 6, 016,280) in view of Sakata et al. (U.S. Patent No. 5,606,265). The Office Action takes the position that the combination of Maesako and Sakata teach or suggest all the features recited in claims 8-10, 13, and 14. Applicants respectfully disagree.

Claim 8 is directed to a semiconductor memory device comprising a SRAM memory block provided on a chip. The SRAM memory block includes a first power pad and a SRAM cell array connected to the first power pad. A DRAM memory block is also provided on the chip. The DRAM memory block includes a second power pad and a DRAM cell array connected to the second power pad. A control unit controls the on/off of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used.

Claim 13 recites a semiconductor memory device comprising a SRAM memory block provided on a chip, the SRAM memory block includes an SRAM cell array. A DRAM memory block is also provided on the chip. The DRAM memory block has a DRAM cell array. A control unit is connected to each of the SRAM memory block and the DRAM memory block. The control unit includes a first pad and a second pad. The control unit activates an operation of one of the SRAM memory block or the DRAM memory block based on a combination of a control value indicated by a first control signal presented to the first pad and a second control value indicated by a second control signal presented to the second pad. The control unit activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is deactivated when the DRAM cell array is not used.

The essence of the claimed invention as recited in claims 8 and 13, is a control unit controlling the ON/Off of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM memory cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used, and a control unit that activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is

deactivated when the DRAM cell array is not used. The benefits provided by the claimed invention include reducing the power consumption of the semiconductor memory device when the DRAM is not used. Further, the claimed invention makes it possible for the same memory address to be assigned to the SRAM cell array and the DRAM cell array. Also, the claimed invention avoids the increase in the cost of the SRAM only system while meeting the demands of large memory system, and in reducing the power consumption of the entire system to a level lower that the power consumption level of the DRAM only system. Accordingly, it is submitted that the prior art fails to disclose or suggest the features of the Applicants' invention.

Maesako discloses a semiconductor memory device that includes a power source voltage converter circuit 603 which generates a first internal power source voltage VINT1 and a second internal power source voltage VINT2 on the basis of an external power source voltage VEXT. The first internal power source voltage is applied to the DRAM array portion and the second internal power source voltage is applied to the SRAM array portion. However, Maesako does not teach or suggest controlling On/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used. Further, the first and second internal power source voltages VINT1 and VINT 2 are not the same as the power pads as recited in the claimed invention. The first and second internal power source voltages are generated by the voltage converter circuit 603 on the basis of an external power source voltage VEXT. In contrast, the claimed invention the power pads of the claimed invention are separately provided for supplying power to the SRAM and DRAM memory block. Maesako, however, utilizes the external power source voltage VEXT in the SRAM array portion. As a result, the objective of Maesako is not the same as the claimed invention. In other words, Maesako does not teach or suggest the benefit of reducing the power consumption of the semiconductor memory device when the DRAM is not used to retain data. Thus, it is submitted that Maesako neither teaches nor suggests all the features of the claimed invention. Furthermore, it is also submitted that Sakata does not cure the deficiencies of the Maesako.

Sakata discloses a process to reduce the power dissipation of a semiconductor

integrated circuit chip when it is operated at an operating voltage of 2.5 V or below. More specifically, Sakata discloses that the dissipation current of the non-active circuit blocks can be reduced while the active current is caused to flow in the active circuit blocks. The source voltage supplied to the circuit blocks that can be cut off is limited to a certain circuit portion, which does not cover the entire DRAM memory block. For instance, figure 11 of Sakata illustrates that the power supplied to the inverter INV can be cut off, but the power supplied to the NAND gate located at the preceding portion of the INV cannot be cut off. Thus, Sakata does not teach or suggest the feature of controlling the ON/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array memory block is cut off when the DRAM cell array is not used, as recited in claim 8. Also, Sakata does not teach or suggest a control unit that activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is deactivated when the DRAM cell array is not used as recited in claims 13. Therefore, it is respectfully submitted that the applied references neither teach nor suggest all the features recited in claims 8 and 13. Accordingly, Applicants request the withdrawal of the rejection of claims 8 and 13 under 35 U.S.C 103(a).

It is respectfully submitted that since claims 10, and 14 are dependent upon claims 8 and 13, which recites patentable subject matter. As a result, claims 10 and 14 likewise recite patentable subject matter that is neither taught nor suggested by the applied references. Therefore, Applicants respectfully request the withdrawal of the rejection of claims 10, and 14.

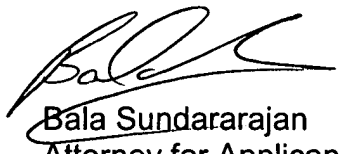
In view of the above amendments and remarks, withdrawal of the rejections to claims 8, 10, 13 and 14 is respectfully requested. Claims 8, 10, and 13 are amended. Claim 9 is cancelled. No new matter is presented. Accordingly, Applicants submit that the claims 8, 10, 13, and 14 recite subject matter that is neither taught nor suggested by the applied prior art. Therefore, Applicants further submit that the application is now in condition for allowance with claims 8, 10, 13 and 14 contained therein.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number

listed below. In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosure: Marked-up Copy of the Claims

Marked-up Copy of the Claims

8. (Amended) A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including a first power pad and an SRAM cell array connected to the first power pad; [and]

a DRAM memory block provided on the chip, the DRAM memory block including a second power pad and a DRAM cell array connected to the second power pad; and

a control unit controlling ON/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used [wherein a source voltage is externally supplied to the DRAM memory block when the DRAM cell array is accessed, and said source voltage to the DRAM memory block is set to a ground voltage when the DRAM cell array is not accessed]

10. (Amended) The semiconductor memory device of claim 8, wherein [further comprising: a power pad shared b the SRAM memory block and the DRAM memory block, the power pad receiving the externally supplied source voltage; and a control unit for controlling] the control unit controls ON/OFF of the source voltage supplied [from the power pad] to the entire DRAM memory block in response to a control signal which is externally supplied to the control unit.

13. (Amended) A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array;

a DRAM memory block provided on the chip, the DRAM memory block having a DRAM cell array; and

a control unit connected to each of the SRAM memory block and the DRAM memory block, the control unit including a first pad and a second pad, the control unit activating an operation of one of the SRAM memory block or the DRAM memory block based on a combination of a first control value indicated by a first control signal

presented to the first pad and a second control value indicated by a second control signal presented to the second pad,

wherein the control unit activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is deactivated when the DRAM cell array is not used.